

LT7642GX --- Product Brief

HDMI2.1/DP1.4 with Type-C to HDMI2.1 and Quad-port MIPI/LVDS Mixed Switch

1. Features

HDMI2.1 RX&TX

- Compliant with HDMI2.1, HDMI2.0b, HDMI1.4 and DVI1.0
- Data rate up to 12Gbps
- Support HDCP 1.4/2.3
- Support HDCP repeater
- Support RGB 8/10/12 bpc, YCbCr4:4:4/ YCbCr4:2:2/ YCbCr4:2:0 8/10/12 bpc
- Support HDR10
- Support FEC
- Support CEC
- Support VRR
- Integrated EDID shadow (max 512-byte)
- Support ARC RX
- Support EARC RX
- Support lane swap and PN swap

USB Type-C

- Compliant with VESA DisplayPort Alt Mode on USB
 Type-C Standard 1.0b
- DP Alt Mode support pin assignment C and E
- Compliant with USB power delivery specification 3.0
- Compliant with USB Type-C cable and connector specification 1.3
- Built-in dual CC logic and PD controller for charger and normal communication
- Data roles supported: UFP and DFP
- Power roles supported: source, sink and DRP
- Support USB Billboard

DP1.4a/eDP1.4b Receiver

 Compliant with DisplayPort specification 1.4a for 1.62Gbps, 2.7Gbps, 5.4Gbps and 8.1Gbps

- Compliant with Embedded DisplayPort specification version 1.4b
- Support SSC
- Support DisplayPort 1/2/4 lanes
- Support ASSR for eDP
- Support HDCP 1.3/2.3
- Support HDCP repeater
- Support SST mode
- Support RGB 6/8/10/12 bpc, YCbCr4:4:4/YCbCr4:2:2/ YCbCr4:2:0 8/10/12 bpc
- Support HDR10
- Support Adaptive-Sync
- Support Horizontal Blanking Expansion

Digital Audio Input and Output

- I2S interface supports up to 8-channel audio, with sample rates of 32~192 KHz and sample sizes of 16~24 bits
- TDM interface supports up to 8-channel audio, with sample rates of 32~192 KHz and sample sizes of 16~24 bits
- SPDIF interface supports LPCM, Dolby Digital, DTS digital audio up to 192KHz frame rate
- Compliant with IEC60958 or IEC61937

● Four-Port MIPI® DSI/CSI Transmitter

- Compliant with D-PHY1.2 & DSI 1.3 & CSI-2 1.3; 1
 clock lane, and 1/2/3/4 configurable data lanes;
 2.5Gbps per data lane
- Compliant with C-PHY1.0 & DSI-2 1.0 & CSI-2 2.0;
 1/2/3 configurable data trio; 2.5Gsps per data trio
- Support 1/2/4 configurable ports
- Support only 1 port for CSI D-PHY 8-lane mode
- Support overlap mode
- DSI Support 16/20/24-bit YCbCr4:2:2, 16/18/24/30-bit
 RGB



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- CSI Support RGB888/666/565, YUV422 8/10bit, YUV420 8bit(legacy)
- Support side by side 3D
- D-PHY support port swap, lane swap and PN swap
- C-PHY support port swap and trio swap

Four-Port LVDS Transmitter

- Compatible with VESA and JEIDA standard
- Support 1/2/4 configurable ports
- 1 Clock lane and 3/4/5 configurable data lanes
- Data rate up to 1.2Gbps per data lane
- Support up to 8K@30Hz YCbCr422 8bit
- Support up to 4K@120Hz YCbCr422 8bit
- Support up to 4K@60Hz RGB 10bit
- Support side by side 3D
- Programmable transmitter swing
- Support SSC
- Support lane swap and PN swap

Resolution

- HDMI2.1 supports up to 4K@144Hz RGB 8bpc, 8K@30Hz RGB 10bpc or 8K@60Hz DSC pass-through
- DP Receiver supports up to 4K@120Hz RGB 8bpc with reduced blanking,4K@144Hz YCbCr422 8bit or 8K@30Hz RGB 8bpc with reduced blanking

• OSD

- Support font-based and bit-map OSD
- Support up to two separate OSD windows
- Support non-rectangular display
- Support adjustable transparency
- Support copying windows in 3D mode

Miscellaneous

- CSC: RGB <-> YCbCr4:4:4 <-> YCbCr4:2:2<-> YCbCr4:2:0
- Integrated 100/400KHz I2C slave
- Integrated microprocessor
- External oscillator 25MHz, +/-50ppm
- Embedded SPI flash for firmware and HDCP keys
- Firmware update through AUX, SPI, I2C or USB interface
- Power supply: 3.3V and 1.1V

2. General Description

LT7642GX is a high performance HDMI2.1 or DP1.4a with Type-C to HDMI2.1 and MIPI/LVDS mixed switch chip for Display application.

HDCP RX as the upstream of HDCP repeater, can cooperate with HDCP TX of other chips to realize the repeater function.

For HDMI2.1 input, LT7642GX can be configured as 3/4 lanes. Adaptive equalization makes it suitable for long cable application and the maximum bandwidth up to 48Gbps.

For HDMI2.1 output, LT7642GX can be configured as 3/4 lanes. The maximum bandwidth is up to 48Gbps.

Both HDMI2.1 input and output allow for the highest resolutions of 8K@30Hz, 4K@144Hz or 8K@60Hz with compression data.

The Type-C/DP1.4a input support data rate up to 8.1Gbps be configured as 1/2/4 lanes. Adaptive equalization makes it suitable for long cable application and the maximum bandwidth is up to 32.4Gbps.

For MIPI output, LT7642GX features configurable single-port or dual-port or quad-port MIPI®DSI/CSI with 1 high-speed clock lane and 1~4 high-speed data lanes operating at maximum 2.5Gbps/lane with D-PHY, which can support a total bandwidth of up to 40Gbps for four port. LT7642GX also support 2.5Gsps/trio with C-PHY, which can support a total bandwidth of up to 68.4Gbps for four port.

For LVDS output, LT7642GX can be configured as single, dual or quad-port LVDS with 1 high-speed clock lane, and 3~5 high-speed data lanes, operating at maximum 1.2Gbps per lane, which can support a total bandwidth of up to 24Gbps. LT7642GX supports flexible video data mapping path for 2D and 3D applications.

Digital audio output interfaces are available, including I2S/TDM/SPDIF. Two digital audio input interfaces are available, including I2S/SPDIF.

The device is capable of automatic operation which is enabled by an integrated microprocessor that uses an embedded SPI flash for firmware storage. System control is also available through the configuration I2C slave interface.



3. Applications

- Mixed Switch
- Mobile system
- Display
- Video capture
- Video conferencing

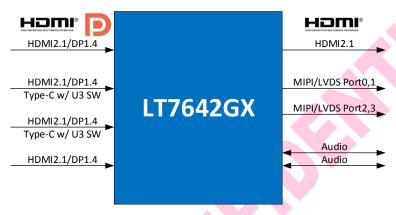


Figure 3.1 Application Diagram

4. Ordering Information

Table 4.1 Ordering Information

| Product Name | Part Number | Product Status | Package | Bonding Wire | Grade | Operating Temperature Range | Stack Die Option | Packing Method | MPQ |
|-----------------|-------------------|-------------------|-------------------|-----------------|-------|-----------------------------------|------------------------|-------------------|-----|
| LT7642GX | LT7642GX_U1B03CEM | Preview | BGA288 (12*12) | Cu | Е | -40°C to +85°C | М | Tray | TBD |

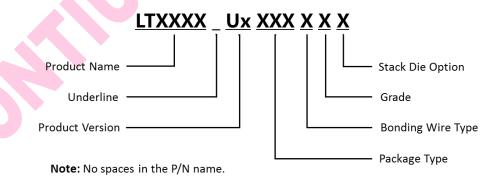


Figure 4.1 Part Number Naming Rules



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