

LT86101SX ADVANCE INFORMATION – CONFIDENTIAL AND PROPRIETARY

LT86101SX --- Product Brief HD-DVI/DVI Repeater

1. Features

- Compatible with HD-DVI 1.3, supports 2.25Gbps data rate
- Support 1080p@60Hz video resolution and 3D video formats
- Support deep color
- Adaptive receive equalization up to 40dB to compensate for long/cheap cable losses
- ODTs and calibration for better signal integrity
- Separate ODT supply for AC-coupled applications
- Configurable transmit de-emphasis up to -9dB to pre-compensate signal distortion
- Integrated back-termination to improve output signal quality
- 5V-tolerant active DDC buffer allowing capacitance up to 3000pF
- Parallel active CES (Consumer Electronics Service) buffer with drive capability up to 3000pF
- Extends cable length as follows: (RX-side + TX-side)
 - Up to (55m + 20m) over 26 AWG STP HD-DVI cable @ 1.65Gbps
 - Up to (35m + 20m) over 26 AWG STP HD-DVI cable @ 2.25Gbps
 - Up to (25m + 15m) over 28 AWG STP HD-DVI cable @ 1.65Gbps
 - Up to (15m + 10m) over 28 AWG STP HD-DVI cable @
 2.25Gbps
- Cascadable for further cable reach
- Dual control modes for flexible applications
- Link activity detection to enable squelch option
- Power dissipation of 0.75W typical
- 7mm x 7mm 48-pin QFN lead-free package

2. General Description

The LT86101SX is Lontium's 4th generation HD-DVI/DVI repeater based on ClearEdge[™] technology, compliant

with the HD-DVI 1.3 specification. It is a 6.75Gbps (3 x 2.25Gbps) high performance re-clocking device that supports 3 TMDS data channels and a single clock channel. The device also integrates a bi-directional DDC active buffer and a parallel CES (Consumer Electronics Service) active buffer to provide a complete HD-DVI/DVI repeater solution.

The LT86101SX incorporates an adaptive receive equalizer, a clock and data recovery (CDR) circuit and a de-emphasis driver on each TMDS data channel. The clock channel feeds a high-performance phase-locked loop (PLL) that regenerates a low jitter output clock. The receive equalizer analyzes the incoming data signal and automatically determines the amount of equalization to compensate the attenuation caused by long HD-DVI/DVI cables and FR4 traces. The CDR circuit retimes the equalized data, incorporated with PLL, to create clean clock and data outputs, reducing both deterministic and random jitter. This low level of output jitter provides system designers with extra margin and flexibility when working with stringent timing budget or long-cable applications. Also, several devices can be cascaded to extend cable reach without degrading signal fidelity. The transmitter supports configurable transmit de-emphasis so that the output can be optimized for driving additional lengths of cables or FR4 traces.

For better signal integrity, ODTs and calibration circuit are implemented in the receiver. Furthermore, offset existing on the receiver path can be automatically cancelled. The transmitter can operate at standard current level, or operate at 50% higher current level to support back-termination to achieve high return loss. This effectively improves the output signal quality due to impedance discontinuity.

The active DDC and CES buffer bi-directionally restores signal integrity of DDC and CES buses. The DDC buffer

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features compensation for cable capacitance with a range from 300pF to 3000pF on source side, and from 150pF to 1500pF on sink side. The slew-rate-limited driver prevents DDC bus from ringing and mutual coupling. The DDC buffer has parallel and serial mode. In serial mode, it isolates capacitances of source side and sink side, with the limitation of un-cascadable characteristic. While in parallel mode, the buffer can be cascaded, but total capacitive loading also can be seen by both source device and sink device. Besides, the buffer can de-skew the two bus-line delays to compensate or adjust the marginal timing due to unbalanced propagation paths or bad I2C master behavior. The CES buffer has only parallel mode because of the requirement of CES line connectivity specification. It provides 3000pF drive capability, and compliant with CES line degradation off-leakage specification when the chip is in the power off state.

Dual control modes are available for LT86101SX. This provides system designers with very flexible solutions, for

consideration of either performance or cost. The LT86101SX supports two control modes: Pin Control Mode and I2C Control Mode. In Pin Control Mode, no external MCU is needed, and the basic functions are under control of pin configurations, however advanced functions are at default settings. In I2C Control Mode, an external MCU is required, and the chip is fully controlled by MCU while the control pin configurations are not valid any more.

The LT86101SX is offered in a 7mm x 7mm 48-lead QFN package, and operates over a -40°C to +85°C temperature range.

3. Applications

- TMDS cable equalizer
- HD televisions and displays
- DVI/HD-DVI cable-extender modules
- Cable assemblies

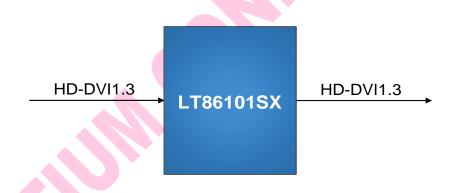


Figure 3.1 Application Diagram

4. Ordering Information



Part Number	Operating Temperature Range	Package	Packing Method	MPQ
LT86101SX	-40°C to +85°C	QFN48 (7*7)	Tray	2600pcs



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